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REMARKS/ARGUMENTS

Reconsideration and allowance of the subject application are respectfully requested.

The Examiner requests that the blocks in Figure 5 be labeled. A replacement sheet for Figure 5 is attached with this response providing the requested labels. Support for those labels is found on page 16, lines 17-20.

All claims stand rejected under 35 USC §102(a) as being anticipated by "Hardware Development of μPLAT" by Kishi et al. This rejection is respectfully traversed.

To establish that a claim is anticipated, the Examiner must point out where each and every limitation in the claim is found in a single prior art reference. *Scripps Clinic & Research Found. v. Genentec, Inc.*, 927 F.2d 1565 (Fed. Cir. 1991). Every limitation contained in the claims must be present in the reference, and if even one limitation is missing from the reference, then it does not anticipate the claim. *Kloster Speedsteel AB v. Crucible, Inc.*, 793 F.2d 1565 (Fed. Cir. 1986). Kishi fails to satisfy this rigorours standard.

In Figure 1, Kishi discloses a processor core design termed the μPLAT® core. By using this core, system LSIs (i.e., large scale integrations of other system components onto the core platform) can be efficiently integrated. Figure 2 is an integrated system which is a complete hardware system with a fixed design. As described in section 4.2,

Figure 4 illustrates a simulation environment for such an integrated system and shows the integrated system of Figure 2 surrounded by a testbench. ARM Limited's Software Development Toolkit (SDT) is used to produce a test program which can then be run on the integrated system. Both the integrated system and the testbench are fixed designs.

A configuration file is coupled to the testbench. Kishi does not describe how this configuration file is used or any details about it. Nevertheless, since the SDT is an ARM product of which the inventor has a working knowledge, the inventor believes that the configuration file is used as follows. The source file(s) for the test program are stored as the C,Asm.file in Figure 4, and this is then compiled by the SDT to produce program/parameter files which are stored as indicated in the top right of Figure 4. The configuration file appears to be used in that compilation process to provide values for certain variables in the source files. This might enable some test program tailoring for the integrated system being tested.

The Examiner infers a great deal from a very small portion of Kishi. Indeed, the Examiner relies solely on Figure 4 and the associated eight lines of description provided in section 4.2 of Kishi (see page 26, right-hand column). Moreover, it is unclear from the Examiner's comments exactly what claim features he believes are disclosed by Kishi. Clarification is requested if the Examiner elects to maintain any rejection based on Kishi.

The Examiner appears to contend that Kishi's whole integrated system corresponds to the "device" in claims 1 and 18 and that the external memory bus in

Figure 4 corresponds with the "bus" in claims 1 and 18. But given Kishi's lack of disclosure about how the configuration file is used, Kishi fails to disclose that the configuration file in Figure 4 contains "predetermined parameters identifying the type of device and capabilities of the device." Further, given that both the testbench and the integrated system are of a fixed design, Kishi also fails to disclose step (b) of claim 1:

> employing a configuration engine to dynamically generate a test environment for the device by creating selected test components which are coupled via the bus with a representation of the device to form the test environment, the test components being selected dependent on the configuration file.

Element (i) of claim 18 recites similar features. Lacking features recited in the independent claims, Kishi fails to anticipate claims 1 and 18.

The amended preambles of claims 1 and 18 more specifically define the device and the bus and further illustrate why Kishi does not disclose claims 1 and 18. As explained on page 1, lines 6-15 of the application, the present invention concerns the development of components for integration into a system, and in particular, relates to techniques to check that each component interfaces with a bus in accordance with a defined bus specification. Example device types which may be tested include master, slave, arbiter, decoder, etc. Each device type will be understood by a person skilled in the art to be a system subcomponent. Figure 1 shows a System-on-Chip (SoC) example in which such devices may be incorporated. The SoC includes a system bus 110 and a

peripheral bus 195 (see page 11, lines 12-13). The device to be tested is a component of a System-on-Chip, and the bus is within the System-on-Chip.

Kishi does not describe a method for testing device compliance with a bus protocol, where the device is a component internal to the integrated system. For example, with reference to Kishi's Figure 2, such a bus includes the expanded system bus or the expanded peripheral bus. But this detailed structure within the integrated system is not directly tested in Kishi. The details of the individual devices within the integrated system are hidden to the testbench illustrated in Figure 4 of Kishi. Thus, Kishi does not disclose "reading a configuration file containing predetermined parameters identifying the type of the device and the capabilities of the device" because Kishi's configuration file does not specify such parameters.

Nor does Kishi teach dynamic generation of a test environment because Kishi's test environment is fixed. Kishi's test environment incorporates the logic components of Figure 2 provided within the grayed box. The "device" corresponds to one or more of the μPLAT® core components shown in the upper left corner of Figure 2. Because Kishi's system is a fixed hardware design and the test environment is fixed, Kishi does not employ a configuration engine to dynamically generate a test environment for the device by creating selected test components. In contrast, Kishi's test components, i.e., one or more of the grayed boxes shown connected to the expanded system bus or the expanded peripheral bus, are fixed pieces of hardware. Finally, the test components in Kishi are not selected depending on the configuration file, as required by claims 1 and 18. This further

confirms that the claimed configuration file is entirely different to the configuration file illustrated in Figure 4 of Kishi.

Because Kishi's testbench has no exposure to the internal workings of the integrated system that it surrounds, Kishi fails to disclose:

> monitoring signals passed between the representation of the device and one or more of the test components during execution of the test sequence to generate result data indicated compliance with the bus protocol.

The bus protocol relates to the bus provided within the System-on-Chip, for example, the expanded system bus or expanded peripheral bus illustrated in Kishi's Figure 2. The test environment in Kishi's Figure 4 has no way of monitoring signals passed over those buses between the device and one or more of the test components because they are provided internally to the integrated system. Accordingly, Kishi has no way of generating result data indicating compliance with the bus protocol.

For the reasons set forth above, Applicant respectfully submits that the present application is now in condition for allowance. An early notice to that effect is earnestly solicited.

Respectfully submitted,

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Attachment: Replacement Sheet(s)